THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 28

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte YOSHIYUKI MIYAYAMA and CHENG-LONG TANG

_____

Appeal No. 96-0576
Application 07/846,231[1]

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HEARD: November 13, 1997

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Before THOMAS, FLEMING and TORCZON, ***Administrative Patent Judges***.

FLEMING, ***Administrative Patent Judge***.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1 through 9, all of the claims present in the application.

[1]Application for patent filed March 6, 1992.

The invention relates to a system and method for sending simultaneous READ/WRITE requests to at least two subsystems and subsequently canceling the request not needed. Appellants disclose on pages 10 through 12 of the specification with reference to Figures 1, 3B and 5, that when code 310 of an instruction is decoded by IPU 105 and when operation code 310 indicates that an access to one of the resources, IOU 130 or MCU 120, is required, each of the resources, IOU 130 or MCU 120, is immediately activated by sending to both IOU 130 and MCU 120 a READ/WRITE request 520. When the remainder of the instruction is decoded by MCU 120 and it is determined which of the resources, either IOU 130 or MCU 120, is needed to be accessed, the MCU 120 issues a cancellation signal. If it is determined that the IOU 130 is performing the READ/WRITE operation, the MCU 120 issues a cancellation signal to itself to cancel its own READ/WRITE request. If it is determined that the MCU 120 is performing the READ/WRITE operation, the MCU 120 issues a cancellation signal to IOU 130 to cancel the IOU 130 READ/WRITE request.

The independent claim 1 is reproduced as follows:

> 1. A method for reducing the critical path in a processor based system during READ/WRITE operations, the system having a memory control unit (MCU), an Input/OutPut control unit (IOU) and an instruction set comprising the steps of:

(a) decoding a first part of an instruction from the instruction set;

(b) determining if said instruction requires at least one of a READ and a WRITE operation;

(c)sending a request to both the MCU and the IOU to enter the READ/WRITE state if it is determined in step b that a READ and/or a WRITE is required;

(d) decoding the remainder of the instruction to determine the address(es) to be accessed by the READ and/or WRITE operation;

(e) decoding the address(es) to be accessed, the decoding performed by at least one of the MCU and the IOU to determine whether the access is directed toward memory or I/O devices; and

(f) cancelling one of said requests to the MCU and IOU based on the results of said decoding step (e).

The Examiner relies on the following references:

Stinson et al. (Stinson) 4,757,439 July 12, 1988

Claims 1 through 9 stand rejected under 35 U.S.C. § 103 as being unpatentable over Stinson.

Rather than reiterate the arguments of Appellants and the Examiner, reference is made to the briefs[2] and answer for the

[2]Appellants filed an appeal brief on January 27, 1995. We will refer to this appeal brief as simply the brief. Appellants filed a reply appeal brief on July 10, 1995. We will refer to this reply appeal brief as the reply brief. The Examiner responded to the reply brief with a letter, mailed August 16, 1995, stating that the reply brief has been entered and considered but no further response by the Examiner is deemed

respective details thereof.

OPINION

We will not sustain the rejection of claims 1 through 9 under 35 U.S.C. § 103.

The Examiner has failed to set forth a ***prima facie*** case. It is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed invention by the express teachings or suggestions found in the prior art, or by implications contained in such teachings or suggestions. ***In re Sernaker***, 702 F.2d 989, 995, 217 USPQ 1, 6 (Fed. Cir. 1983). "Additionally, when determining obviousness, the claimed invention should be considered as a whole; there is no legally recognizable 'heart' of the invention." ***Para-Ordnance Mfg. v. SGS Importers Int'l, Inc.***, 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995), ***cert. denied,*** 117 S.Ct. 80 (1996) ***citing W. L. Gore & Assocs., Inc. v. Garlock, Inc.***, 721 F.2d 1540, 1548, 220 USPQ 303, 309 (Fed. Cir. 1983), ***cert. denied***, 469 U.S. 851 (1984).

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necessary.

Appellants argue on pages 9 through 13 of the brief that Stinson fails to teach or suggest decoding a first part of an instruction to determine if a READ or a WRITE operation is required and if such operation is required sending to the system resources a request to place these resources in a READ/WRITE state. Appellants further argue that Stinson fails to teach or suggest that once the remainder of the instruction is decoded, and it is determined which resource is to be accessed, the requests to the other resources are canceled. Appellants further emphasize on pages 3 through 5 of the reply brief that Stinson fails to teach the above claimed limitations as recited in Appellants' claims.

We note that Appellants' claim 1 recites in part the following:

> (a) decoding a first part of an instruction from the instruction set;
>
> (b) determining if said instruction requires at least one of a READ and a WRITE operation;
>
> (c) sending a request to both the MCU and the IOU to enter the READ/WRITE state if it is determined in step b that a READ and/or a WRITE is required;
>
> (d) decoding the remainder of the instruction to determine the address(es) to be accessed by the READ and/or WRITE operation;

(e) decoding the address(es) to be accessed, the decoding performed by at least one of the MCU and the IOU to determine whether the access is directed toward memory or I/O devices; and

(f) canceling one of said requests to the MCU and IOU based on the results of said decoding step (e).

We note that Appellants' claim 4 recites in part the following:

(a) decoding a first part of an instruction from the instruction set;

(b) determining if said instruction requires an access operation;

(c) sending a request to at least two of the resources to enter an access state if it is determined in step b that access to the resources is required;

(d) decoding the remainder of the instruction to determine the address(es) to be accessed;

(e) decoding the address(es) to be accessed, decoding performed by at least one of the resources to determine which of said at least two of the resources will be accessed; and

(f) canceling the remainder of the requests based on the results of said decoding step (e).

Finally, we note that Appellants' only remaining independent claim, Appellants' claim 7, recites in part the following:

(a) means for decoding a first part of an instruction from the instruction set;

(b) means for determining if said instruction requires an access operation;

> (c) means for sending a request to at least two of the resources to enter an access state if it is determined by said means for determining that access to the resources is required;
>
> (d) means for decoding the remainder of the instruction to determine the address(es) to be accessed;
>
> (e) means for decoding the address(es) to be accessed, decoding performed by at least one of the resources to determine which of said at least two of the resources will be accessed; and
>
> (f) means for canceling the remainder of the requests based on the results of the decoded address(es).

Upon a careful review of Stinson, we fail to find that the reference teaches the above limitations as recited in Appellants' claims.

Stinson does teach in column 3, lines 17-22, that the microprocessor 1 shown in Figure 1 has three status lines 13. Furthermore, Stinson teaches in column 4, lines 24- 27, that the microprocessor outputs a status on the status lines 13 to indicate when the microprocessor 1 is reading or writing to memory. However, Stinson is silent as how this status is determined. Stinson fails to teach that the Stinson's microprocessor decodes a first part of an instruction from the instruction set, determines if said instruction requires an access operation and sends a request to at least two of the resources to enter an access state if it is determined that

access to the resources is required as recited in Appellants' claims.

In addition, we note that Stinson does teach in column 4, lines 24-67, that the status of the microprocessor 1 is determined by the Early READ/WRITE logic circuit 12 which determines if the microprocessor 1 is reading or writing to memory. If the Early READ/WRITE logic circuit 12 determines that the microprocessor is reading or writing to memory, the Early READ/WRITE logic circuit 12 sends a memory write (MWT) signal 14

or a memory read (MRD) signal 15 to the memory bus interface 20. When a memory bank receives an appropriate address from the microprocessor 1 and a MRD or MWT signal, the memory bank responds back over the memory bus interface 20 with a RAM acknowledgment signal to signal to the microprocessor 1 that the memory bank will be ready to complete the READ or WRITE cycle. Stinson teaches that this ensures maximum throughput of the unified bus interface during the READ or WRITE operation.

However, Stinson fails to teach decoding the remainder of the instruction to determine the address(es) to be accessed, decoding the address(es) to be accessed, decoding performed by at least one of the resources to determine which of said at least

two of the resources will be accessed and canceling the remainder of the requests based on the results of the decoding of the address(es) as recited in Appellants' claims. The Stinson system is directed to allow the microprocessor 1 and the memory bank to operate synchronously momentarily during a read or write cycle. Stinson does not teach canceling the resources that are not needed for the access operation as recited in Appellants' claims.

Furthermore, we fail to find any suggestion of modifying Stinson's synchronous data transfer system to provide a system having a multiplicity of resources placed in an access state before decoding the instruction to determine the addresses to be accessed and then later canceling this access state for the resource not to be accessed once it is determined which resource is to perform the access operation as recited in Appellants' claims. The Federal Circuit states that "[t]he mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." ***In re Fritch***, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992), ***citing In re Gordon***, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). "Obviousness may not be

established using hindsight or in view of the teachings or suggestions of the inventor." ***Para-Ordnance Mfg.***, 73 F.3d at 1087, 37 USPQ2d at 1239, ***citing W. L. Gore***, 721 F.2d at 1551, 1553, 220 USPQ at 311, 312-13.

Stinson is not concerned with the problem that Appellants' are attempting to solve. Stinson is concerned with the problem of reducing the time to transfer data between a memory and a microprocessor. Stinson solves this problem with an improved memory bus by allowing for momentary synchronous operation during a read or write operation. As pointed out on page 14 of the brief, Appellants's invention is concerned with the problem of the delay due to time required to determine which resource is to

be accessed where the cycle time is driven by the amount of time required to decode the resource address and to transition the address resource to the access state. Because Stinson is not concerned with improving access time for a system which must determine which resource is to be accessed, we fail to find that Stinson provides any reason or suggestion to modify the Stinson momentarily synchronous bus system to the system as claimed by Appellants.

We have not sustained the rejection of claims 1 through 9

under 35 U.S.C. § 103. Accordingly, the Examiner's decision is reversed.

REVERSED

JAMES D. THOMAS Administrative Patent Judge	)	
MICHAEL R. FLEMING Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
RICHARD TORCZON Administrative Patent Judge	)	

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